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Substitute for form 1449A/PTO (Modified by BSTZ 6/30/99) INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known			
		Application Number	101669803		
		Filing Date	9/23/2003		
		First Named Inventor	Simon et al.		
		Group Art Unit	Not Yet Assigned 2111		
Examiner Name	Not Yet Assigned Ave				
Sheet	2	of	4	Attorney Docket Number	42390.P10493

U.S. PATENT DOCUMENTS					
Examiner Initials *	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Filing Date if Appropriate
	Number				
MA		3,619,504	De Veer et al.	11/9/1971	12/24/1969
MA		6,005,895	Perino et al.	12/21/1999	12/20/1996
MA		5,629,838	Knight et al.	5/13/1997	6/24/1994
MA		3,516,065	Bolt et al.	6/2/1970	1/13/1967
MA		5,638,402	Osaka et al.	6/10/1997	9/27/1994

FOREIGN PATENT DOCUMENTS							
Examiner Initials *		Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation? Yes/No
		Office or Country	Number	Date			

OTHER DOCUMENTS			
Examiner Initials *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published (if known).		Translation? Yes/N
MA	XTL Evaluation System Evaluation Memory Sub-System: Chip (HS-TEG: High Speed Test		
MA	Engineering Group) and Dimm, 9/15/2000, Pages 22-35, Volume SDL601-XTL-0-073 DMX 005		
MA	Systems Development Laboratory, Hitachi Ltd.,		
MA	HIDEKI OSAKA, High Performance Memory Interface for DDR-SDRAM II: XTL		
	(Crosstalk Transfer Logic), 9/15/2000, Pages 2-21, Volume SDL601-XTL-0-074 DMX 006		

Examiner Signature	Glen Ave	Date Considered	10/6/2005
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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				Application Number	10 / 669 807
				Filing Date	9/23/2003
				First Named Inventor	Simon et al.
				Group Art Unit	Not Yet Assigned 211
Examiner Name	Not Yet Assigned Anne				
Sheet 3 of 4	Attorney Docket Number 42390.P10493				

U.S. PATENT DOCUMENTS					
Examiner Initials *	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Filing Date if Appropriate
	Number				

FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation? Yes/No
	Office or Country	Number	Date			

OTHER DOCUMENTS		
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MA	Systems Development Laboratory, Hitachi Ltd., RAMIN FARJAD-RAD, ET AL. A 0.3- μ m	
	CMOS-Gb/s 4-PAM Serial Link Transceiver, May 5, 2000, Pages 757-764, IEEE Journal of Solid-State Circuits, Vol. 35, No. 5	
MA	KEN YANG ET AL., A 0.5- μ m CMOS 4.0-Gbits/s Serial Link Transceiver with Data Recover Using Oversampling, May 5, 1998, Pages 713-722, IEEE Journal of Solid-State Circuits, Vol. 33 No. 5	

Examiner Signature: Glenn Anne	Date Considered: 10/6/2005
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